

PH5330

N-channel enhancement mode field-effect transistor

Rev. 02 — 18 July 2003

Product data

1. Description

N-channel enhancement mode field-effect power transistor in a SOT669 (LFAK) package.

Product availability:

PH5330 in SOT669 (LFAK).

2. Features

- Logic level compatible
- Low drive current
- High-density mounting
- Very low on-state resistance.

3. Applications

- DC-to-DC converters
- Computer motherboards
- Switched mode power supplies.

4. Pinning information

Table 1: Pinning - SOT669 (LFAK), simplified outline and symbol

Pin	Description	Simplified outline	Symbol
1,2,3	source (s)		
4	gate (g)		
5	drain (d)		

SOT669 (LFAK)

5. Quick reference data

Table 2: Quick reference data

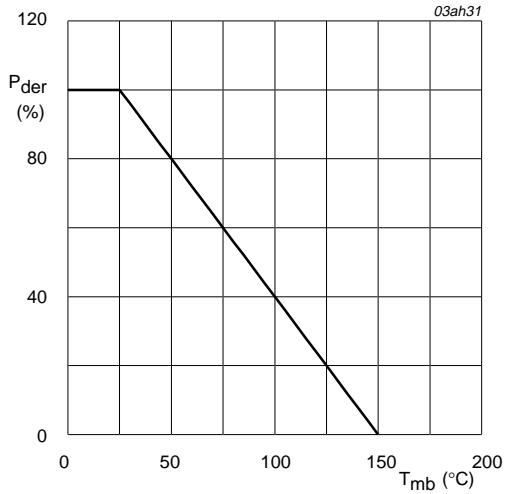
Symbol	Parameter	Conditions	Typ	Max	Unit
V_{DS}	drain-source voltage (DC)	$T_j = 25\text{ °C}$	-	30	V
I_D	drain current (DC)	$T_{mb} = 25\text{ °C}; V_{GS} = 10\text{ V}$	-	50	A
P_{tot}	total power dissipation	$T_{mb} = 25\text{ °C}$	-	39	W
T_j	junction temperature		-	150	°C
R_{DSon}	drain-source on-state resistance	$V_{GS} = 10\text{ V}; I_D = 20\text{ A}; T_j = 25\text{ °C}$	4.6	5.3	mΩ
		$V_{GS} = 4.5\text{ V}; I_D = 20\text{ A}; T_j = 25\text{ °C}$	8.0	10	mΩ

6. Limiting values

Table 3: Limiting values

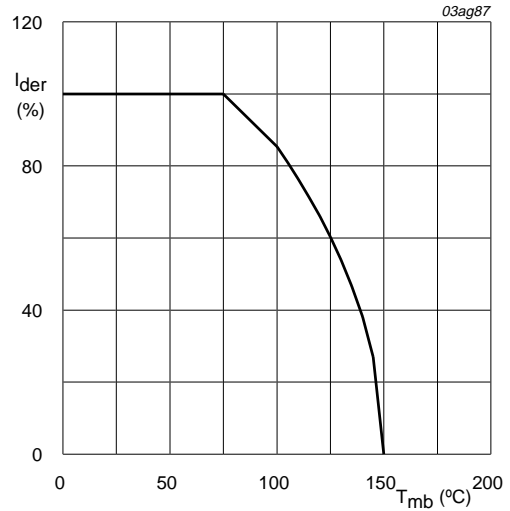
In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Conditions	Min	Max	Unit
V_{DS}	drain-source voltage (DC)	$T_j = 25\text{ to }150\text{ °C}$	-	30	V
V_{GS}	gate-source voltage (DC)		-	±20	V
I_D	drain current (DC)	$T_{mb} = 25\text{ °C}; V_{GS} = 10\text{ V};$ Figure 2 and 3	-	50	A
I_{DM}	peak drain current	$T_{mb} = 25\text{ °C};$ pulsed; $t_p \leq 10\text{ }\mu\text{s};$ Figure 3	-	160	A
P_{tot}	total power dissipation	$T_{mb} = 25\text{ °C};$ Figure 1	-	39	W
T_{stg}	storage temperature		-55	+150	°C
T_j	operating junction temperature		-55	+150	°C
Source-drain diode					
I_{SM}	peak source (diode forward) current	$T_{mb} = 25\text{ °C};$ pulsed; $t_p \leq 10\text{ }\mu\text{s}$	-	50	A



$$P_{der} = \frac{P_{tot}}{P_{tot(25^{\circ}C)}} \times 100\%$$

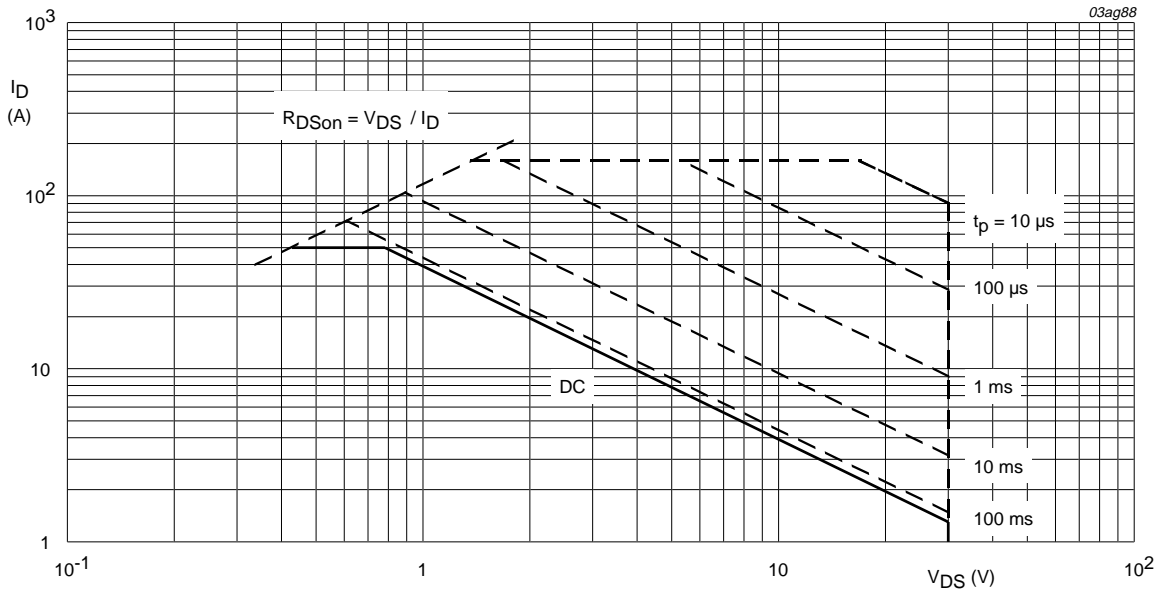
Fig 1. Normalized total power dissipation as a function of mounting base temperature.



V_{GS} ≥ 10 V

$$I_{der} = \frac{I_D}{I_{D(25^{\circ}C)}} \times 100\%$$

Fig 2. Normalized continuous drain current as a function of mounting base temperature.



T_{mb} = 25 °C; I_{DM} is single pulse.

Fig 3. Safe operating area; continuous and peak drain currents as a function of drain-source voltage.

7. Thermal characteristics

Table 4: Thermal characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$R_{th(j-mb)}$	thermal resistance from junction to mounting base	Figure 4	-	-	3.2	K/W

7.1 Transient thermal impedance

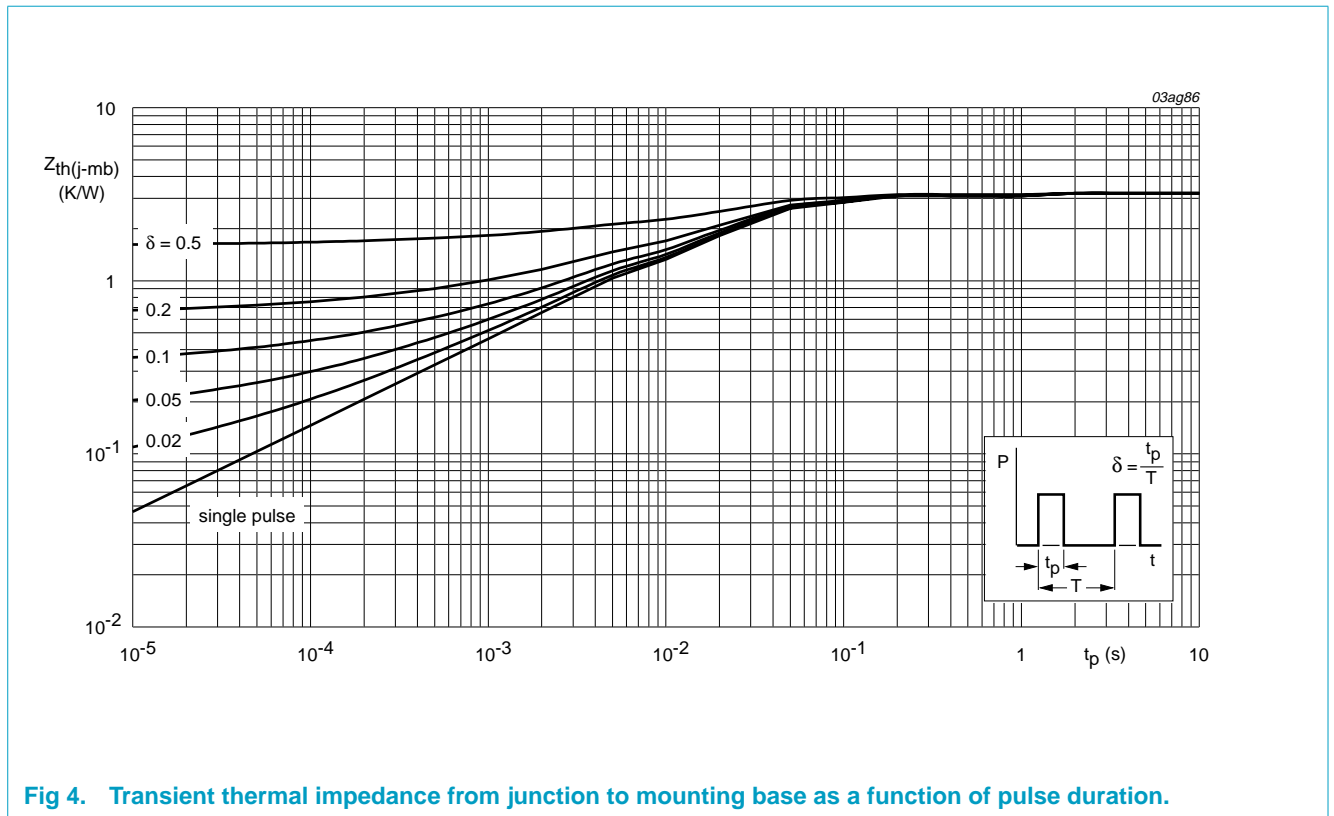


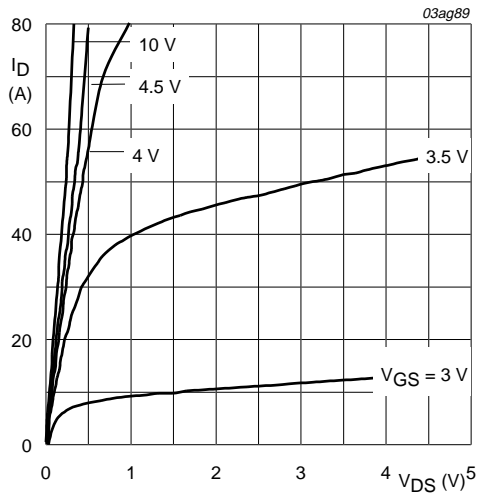
Fig 4. Transient thermal impedance from junction to mounting base as a function of pulse duration.

8. Characteristics

Table 5: Characteristics

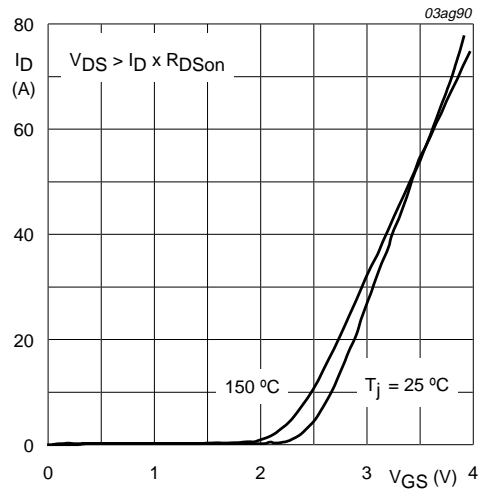
$T_j = 25\text{ }^\circ\text{C}$ unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
Static characteristics						
$V_{(BR)DSS}$	drain-source breakdown voltage	$I_D = 10\text{ mA}; V_{GS} = 0\text{ V}$	30	-	-	V
$V_{GS(th)}$	gate-source threshold voltage	$I_D = 1\text{ mA}; V_{DS} = V_{GS}$; Figure 9	1	1.9	2.5	V
I_{DSS}	drain-source leakage current	$V_{DS} = 30\text{ V}; V_{GS} = 0\text{ V}; T_j = 25\text{ }^\circ\text{C}$	-	0.06	1	μA
I_{GSS}	gate-source leakage current	$V_{GS} = \pm 16\text{ V}; V_{DS} = 0\text{ V}$	-	0.9	10	μA
$R_{DS(on)}$	drain-source on-state resistance	$V_{GS} = 10\text{ V}; I_D = 20\text{ A}$; Figure 7 and 8	-	4.6	5.3	$\text{m}\Omega$
		$V_{GS} = 4.5\text{ V}; I_D = 20\text{ A}$; Figure 8	-	8.0	10	$\text{m}\Omega$
Dynamic characteristics						
g_{fs}	forward transconductance	$V_{DS} = 10\text{ V}; I_D = 20\text{ A}$; Figure 11	30	50	-	S
$Q_{g(tot)}$	total gate charge	$I_D = 40\text{ A}; V_{DD} = 10\text{ V}; V_{GS} = 10\text{ V}$; Figure 14	-	40	-	nC
Q_{gs}	gate-source charge		-	7	-	nC
Q_{gd}	gate-drain (Miller) charge		-	8	-	nC
C_{iss}	input capacitance	$V_{GS} = 0\text{ V}; V_{DS} = 10\text{ V}; f = 1\text{ MHz}$; Figure 12	-	2200	-	pF
C_{oss}	output capacitance		-	600	-	pF
C_{riss}	reverse transfer capacitance		-	330	-	pF
$t_{d(on)}$	turn-on delay time	$V_{DD} = 10\text{ V}; I_D = 20\text{ A}; V_{GS} = 10\text{ V}; R_G = 4.7\text{ }\Omega$	-	20	-	ns
t_r	rise time		-	62	-	ns
$t_{d(off)}$	turn-off delay time		-	59	-	ns
t_f	fall time		-	18	-	ns
Source-drain (reverse) diode						
V_{SD}	source-drain (diode forward) voltage	$I_S = 40\text{ A}; V_{GS} = 0\text{ V}$; Figure 13	-	0.85	1.11	V
t_{rr}	reverse recovery time	$I_S = 40\text{ A}; dI_S/dt = -50\text{ A}/\mu\text{s}; V_{GS} = 0\text{ V}$	-	60	-	ns



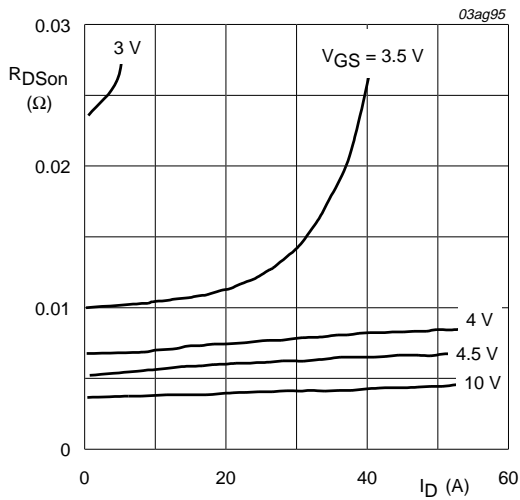
$T_j = 25^\circ\text{C}$

Fig 5. Output characteristics: drain current as a function of drain-source voltage; typical values.



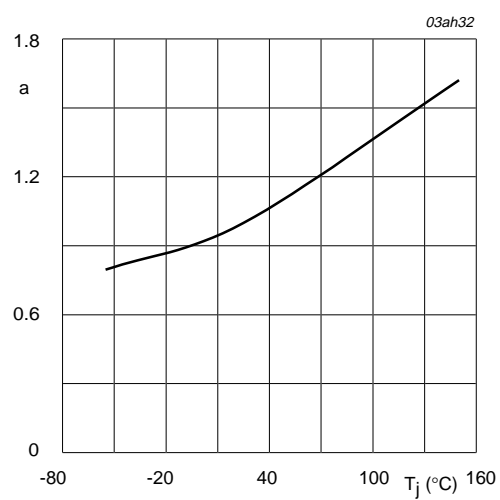
$T_j = 25^\circ\text{C}$ and 150°C ; $V_{DS} > I_D \times R_{DSon}$

Fig 6. Transfer characteristics: drain current as a function of gate-source voltage; typical values.



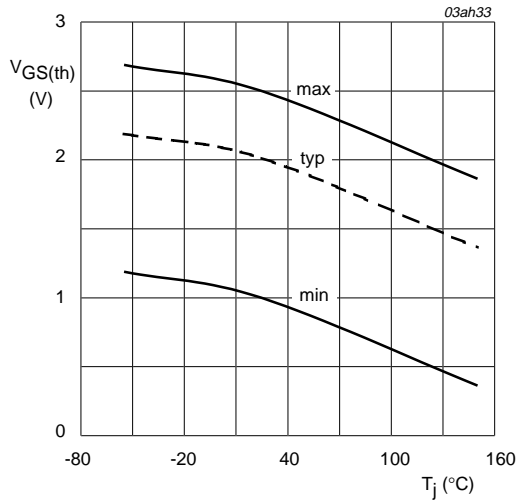
$T_j = 25^\circ\text{C}$

Fig 7. Drain-source on-state resistance as a function of drain current; typical values.



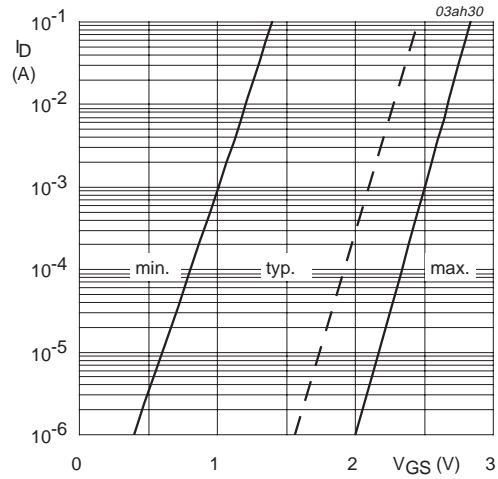
$$a = \frac{R_{DSon}}{R_{DSon(25^\circ\text{C})}}$$

Fig 8. Normalized drain-source on-state resistance factor as a function of junction temperature.



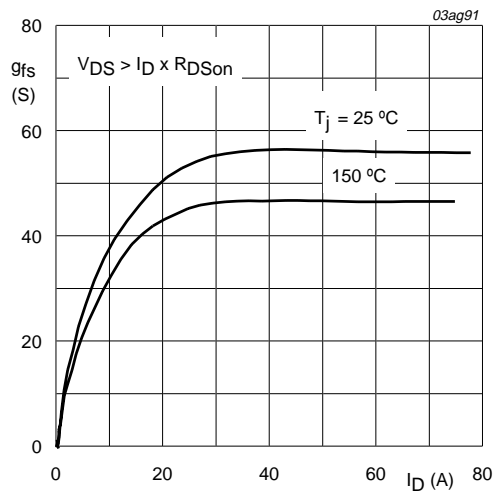
$I_D = 1 \text{ mA}; V_{DS} = V_{GS}$

Fig 9. Gate-source threshold voltage as a function of junction temperature.



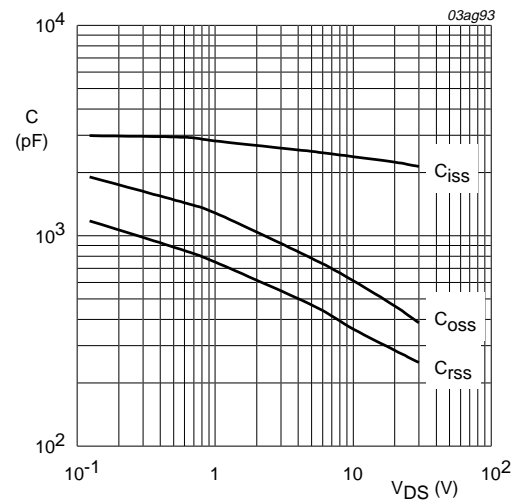
$T_j = 25 \text{ °C}$

Fig 10. Sub-threshold drain current as a function of gate-source voltage.



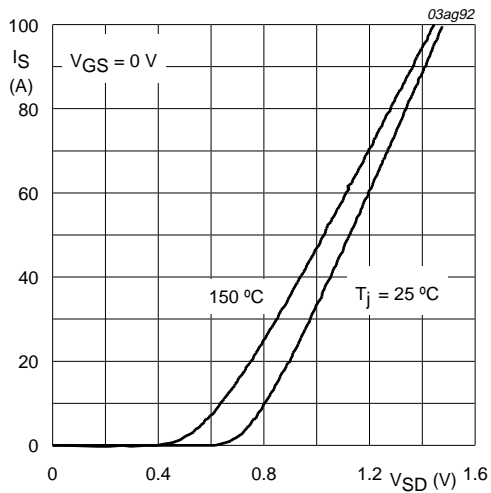
$T_j = 25 \text{ °C and } 150 \text{ °C}; V_{DS} > I_D \times R_{DSon}$

Fig 11. Forward transconductance as a function of drain current; typical values.



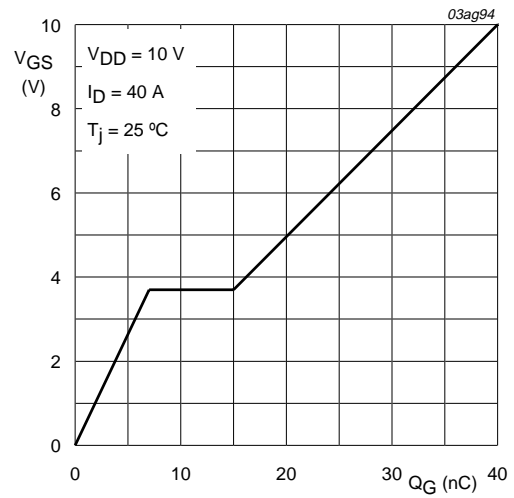
$V_{GS} = 0 \text{ V}; f = 1 \text{ MHz}$

Fig 12. Input, output and reverse transfer capacitances as a function of drain-source voltage; typical values.



$T_j = 25\text{ }^\circ\text{C}$ and $150\text{ }^\circ\text{C}$; $V_{GS} = 0\text{ V}$

Fig 13. Source (diode forward) current as a function of source-drain (diode forward) voltage; typical values.



$T_j = 25\text{ }^\circ\text{C}$; $I_D = 40\text{ A}$; $V_{DD} = 10\text{ V}$

Fig 14. Gate-source voltage as a function of gate charge; typical values.

9. Package outline

Plastic single-ended surface mounted package (Philips version LPAK); 4 leads

SOT669

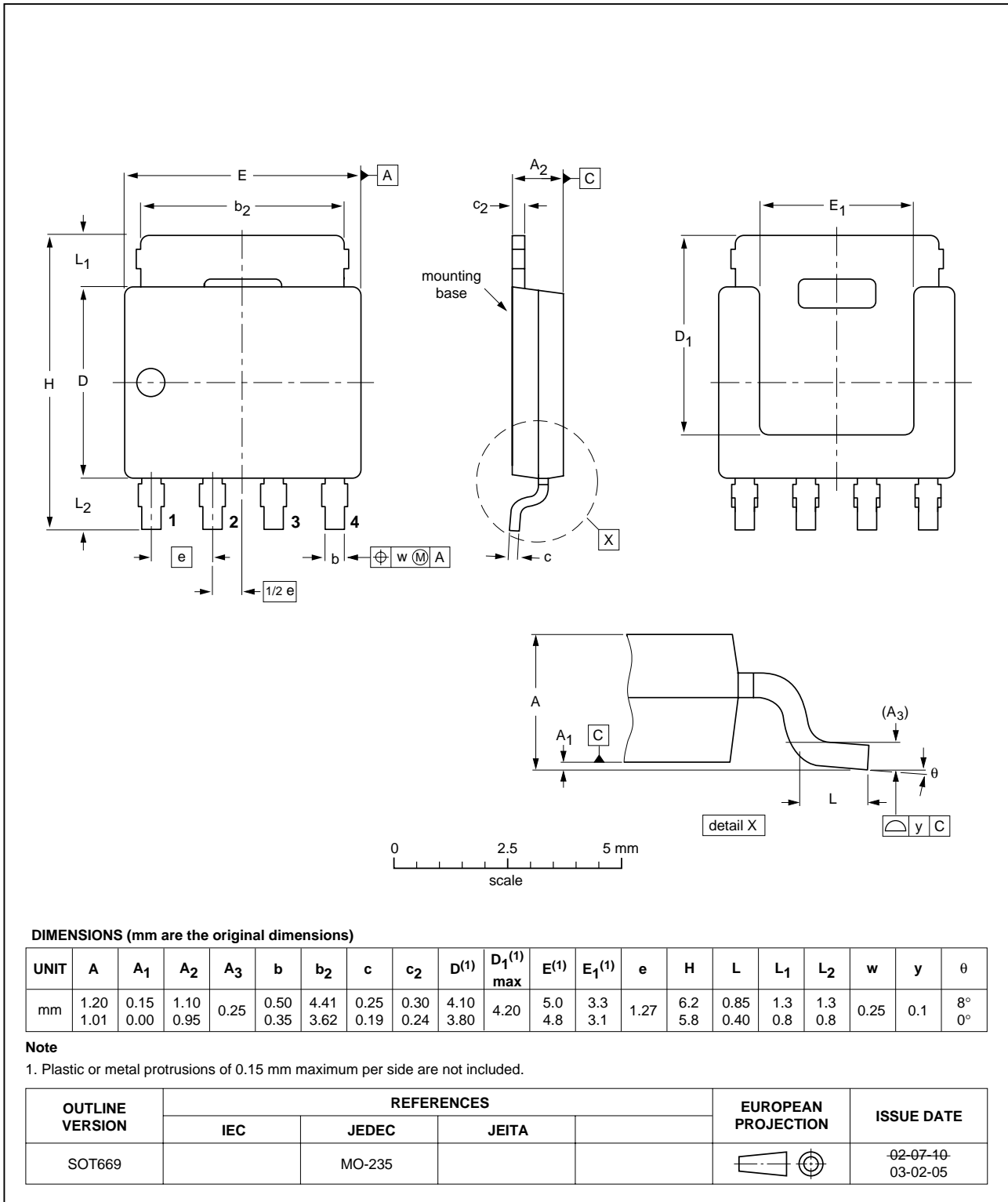


Fig 15. SOT669 (LPAK).

10. Revision history

Table 6: Revision history

Rev	Date	CPCN	Description
02	20030718	-	Product data (9397 750 10951) Modifications: <ul style="list-style-type: none">• JEDEC reference added to package outline drawing in Figure 15
01	20020207	-	Product data (9397 750 09391)

11. Data sheet status

Level	Data sheet status ^[1]	Product status ^{[2][3]}	Definition
I	Objective data	Development	This data sheet contains data from the objective specification for product development. Philips Semiconductors reserves the right to change the specification in any manner without notice.
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